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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DANG, KHANH	
ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/626,756	TRAYNOR ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Specifically, the newly added phrase "based on the assigned priority of the interrupt inputs" (claims 1 and 7) does not have adequate support from the originally filed specification. The only portion of the specification describing the use of "priority" according to Applicants' claimed invention is paragraph [0030], which is reproduced below for ease of reference and convenience.

> **[0030]** The added flexibility afforded through mapping provides many advantages over conventional interrupt-sharing arrangements. Consider, for example, where the IC 340 has assigned priorities to each of the interrupt inputs INT-01 through INT-N. The priority of an interrupt source 310 can be changed dynamically (and repeatedly) by setting the associated control bits to enable requests to be mapped only to the interrupt input having the desired priority level. Moreover, the set of enabled interrupt sources 310 can be changed dynamically according to user preferences, system state, system demands, or a host of other conditions.

If Applicants disagree with the Examiner, Applicants are required to point to the specification by citing page and line number, and to the drawings, for support of the phrase "based on the assigned priority of the interrupt inputs."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wash (5,530,875) in view of Khan et al. (Khan, 6,807,595).

With regard to claim 1, Wach discloses a method for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources, which generates interrupt requests, comprising the steps of: mapping each of the plurality of interrupt sources to each of the plurality of interrupt inputs of an interrupt

controller that receives the interrupt; assigning priorities to each of the plurality of interrupt inputs; and selectively enabling interrupt requests from each of the plurality of interrupt sources to be received at one or more of the plurality of interrupt inputs based on the assigned priorities of the interrupt inputs (Wach discloses an interrupt architecture employing interrupt sharing, which is best illustrated in the following figure:

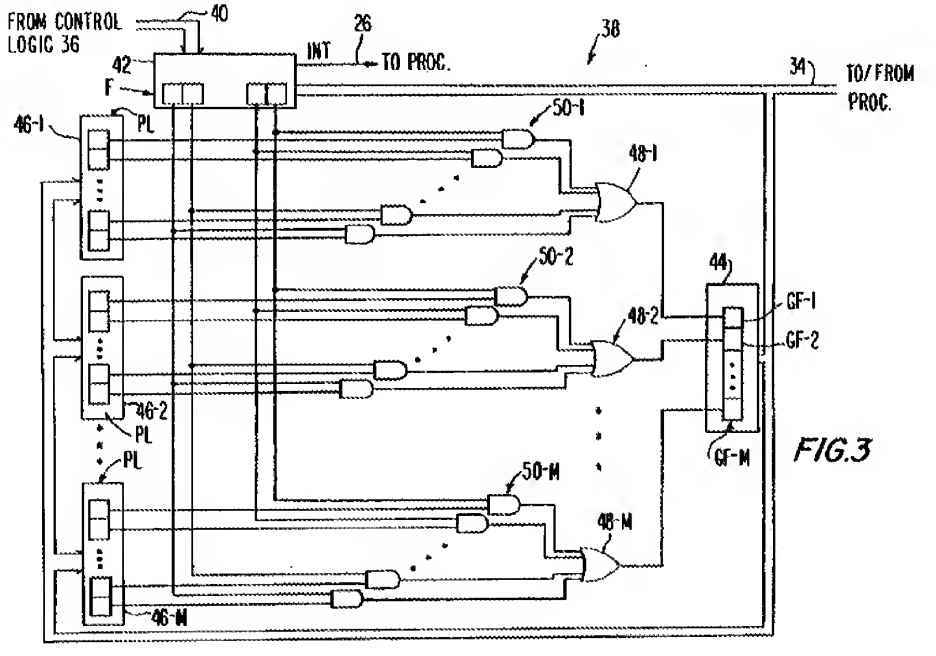

FIG.3

At the outset, in order to have a clear understanding of the following discussion, it is important to note that the interrupt requests can be generated from register 44 instead of register 42 (see column 11, lines 10-15). In addition, the term "group" used in Wash includes group that has only one interrupt resource (see column 11, lines 47-49).

As shown above and specifically described in column 4, line 63 to column 6, line 43; column 10, line 55 to column 11, line 48, the number of storage locations F in register 42 is equal to the number of interrupt sources, any one of which may cause the transmission of the interrupt signal to processor 14. Also, the locations F correspond one-to-one to the interrupt sources. The plurality of interrupt sources are routed or mapped to a plurality of interrupt inputs represented by a plurality of storage locations GF of the group register 44 of the interrupt controller or interrupt manager 38; wherein the interrupt requests are selectively enabled based on the priority of the interrupt inputs. In Wash, as shown in Fig. 3 above, when the interrupt requests from interrupt sources are received at (mapped to) the interrupt inputs GF of the group register 44 of the interrupt controller or manager 38. Further, in Wash, priorities among interrupt sources are established by assigning at least one of the interrupt sources to a first priority group GF1, and assigning the remaining interrupt sources to at least a second priority group GF2. The step of assigning at least one interrupt source to a first priority group includes connecting one of the storage locations F of the interrupt register 42 with one of the storage locations GF of the group register 44. The first group represented by storage location GF1 of group register 44, the second group is represented by storage location GF2 of group register 44. See at least column 2, lines 22-28 and 41-51; column 3, lines 1-10; column 5, lines 2-40; column 6, lines 9-43; column 11, lines 47-49; column 6, lines 48-52; column 10, lines 32-50; claims 1-9.

Thus, it is clear that such a one-to-one connection between each of the interrupt sources (representing by locations F) and each of the interrupt inputs GF of the

interrupt controller 44 is prioritized. In other words, the interrupt inputs GF are selectively enabled by the interrupt controller or manager 38 based on the priorities of the interrupt inputs (priority group GF). Further, in Wash, a masking bit is used to enable or disable interrupt requests from each of a plurality of interrupt sources to one or more of the plurality of interrupt inputs. Specifically, when it is desired to mask a given one of the interrupt sources, processor 14 sends programming signals to the association registers 46 such that the value "0" is stored in the respective location PL corresponding to the interrupt source to be masked).

With regard to claim 2, as discussed above, when it is desired to mask a given one of the interrupt sources, processor 14 sends programming signals to the association registers 46 such that the value "0" is stored in the respective location PL corresponding to the interrupt source to be masked.

With regard to claim 3, as discussed above, when it is desired to mask a given one of the interrupt sources, processor 14 sends programming signals to the association registers 46 such that the value "0" is stored in the respective location PL corresponding to the interrupt source to be masked. Further, as also discussed above, each location PL corresponds to each of interrupt source. Thus, it is clear that a control bit value can be selectively set in each of location PL corresponding to the mapped interrupt source/interrupt input combination.

With regard to claim 4, as discussed above, the masking control bit is programmable. Thus, it is clear that the control bit values can be set according to user preferences.

With regard to claim 5, as discussed above, the masking control bit is programmable. Thus, it is clear that the control bit values can be dynamically modified according to user preferences.

With regard to claim 6, it is clear that the control bit values must be defined according to system requirements. Further, it is also clear that the system of Wash comprises the processor, at least one interrupt source, and at least one interrupt input.

With regard to claims 7-12, see discussion above, since the subject matter presented in claims 7-12 has already been addressed.

With regard to claim 13, as clearly shown in the figure above, the logic that selectively enables comprises, for each mapped interrupt source/interrupt input combination, a logical AND (50) for ANDing each interrupt source with a respective control bit value.

With regard to claim 14, Wash discloses a system for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources (Wach discloses an interrupt architecture employing interrupt sharing, which is best illustrated in the following figure:

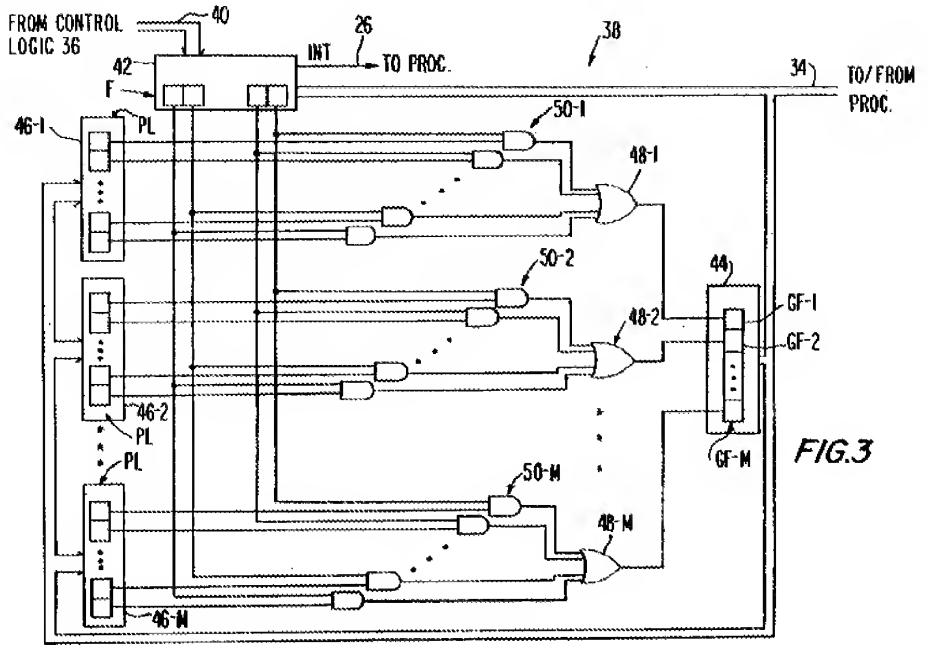

FIG.3

, comprising: for each of said plurality of interrupt inputs: a plurality of logical ANDs, each corresponding to an interrupt source, the corresponding interrupt source providing an interrupt request signal to the corresponding logical AND to interrupt the processor (a plurality of AND gates 50, each having an input to receive an interrupt request signal from an interrupt source to interrupt the processor; see also discussion above regarding claim 1); a plurality of control bits each corresponding to an interrupt source and each respectively providing a control bit value to the corresponding logical AND (a plurality of masking bits, each can be set in the location PL to provide a control value to the other input of AND gate 50; see also discussion regarding claim 1 above), wherein, based on the control bit value, a

corresponding interrupt request signal is provided at an output of the corresponding logical AND (based on the control bit value provided at one input of the AND gate, an interrupt request signal is provided at output of the AND gate 50; see also discussion above regarding claim 1); and a logical OR arranged to indicate, to the interrupt inputs having priority assigned thereto of an interrupt controller that receives the interrupt requests, the presence of a corresponding interrupt request signal from at least one output of the plurality of logical ANDs, wherein the plurality of logical ANDs and operatively connected to the logical OR (as clearly discussed above regarding claim 1, the OR gate 48 is arranged to indicate the presence of a corresponding interrupt request signal from at least one output of the plurality of AND gates 50 to the interrupt input; see also discussion above regarding claim 1).

With regard to claims 15-20, see discussion above, since the subject matter presented in claims 15-20 has already been addressed.

Wash does not specifically disclose that priorities of the interrupt inputs are assigned by the interrupt controller or interrupt manager.

However, using an interrupt controller to assign priorities is old and well-known as evidenced by Khan et al. (Khan, 6,807,595). Khan discloses the use of an interrupt controller for assigning priories instead of using a processor for reducing internal resource. See at least the abstract.

Since Wash and Khan are both from the same field of endeavor, the purpose disclosed by Khan would have been recognized in the pertinent art of Wash.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the interrupt controller of Wash to assign priorities, as taught by at least Khan, for the purpose of reducing internal resource.

Response to Arguments

Applicants' arguments filed 3/3/2008 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997).* As a matter of fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.,* 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The Wach 103 Rejection:

Applicants argued that "The Examiner apparently asserts that Wach's interrupt sources and group flag register 44 correspond to Applicant's claimed "interrupt sources," and "interrupt controller," respectively. (Office Action, p. 5.) Applicant disagrees. Group flag register 44 is a storage device that holds group interrupt flags that are read by a processor 14. (Wach, col. 5:16-18, 6:22-30.) This function of group flag register 44 comports with the plain an ordinary meaning of the term "register," which is "computer circuit that holds values of internal operations." (See, e.g., Answers.com, http://www.-answers.com/topic/status-register?cat=biz-fin, accessed on February 4, 2008.) Thus, group register 44 simply stores data and does not have any control function. As such, group flag register 44 cannot be considered to be an "interrupt controller."

Contrary to Applicants' argument, it is clear that a plurality of location GF of register 44 is readable as a plurality of interrupt inputs; and that register 44 is a part of the interrupt manager 38. As disclosed in [0012], page 4 of Applicants' originally filed specification and as shown in Fig. 3, the interrupt inputs are defined as follows:

[0012] In yet another aspect of the invention, a system is disclosed for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources. The system comprises, for each interrupt input, a plurality of logical ANDs, each corresponding to an interrupt source, the corresponding interrupt source providing an interrupt request signal to the corresponding logical AND to interrupt the processor. A plurality of control bits each correspond to an interrupt source and each respectively provide a control bit value to the corresponding logical AND, wherein, based on the control bit value, a corresponding interrupt request signal is provided at an output of the corresponding logical AND. A logical OR is arranged to indicate, to the interrupt input, the presence of a corresponding interrupt request signal from at least one output of the plurality of logical ANDs.

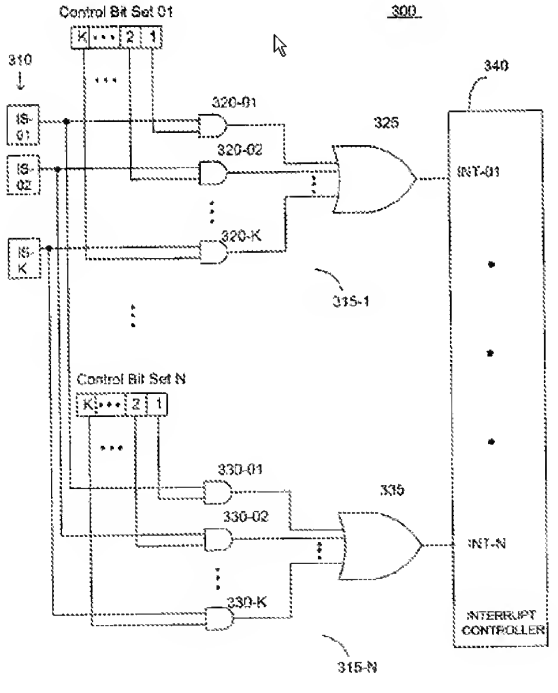

FIG. 3

Identically disclosed and shown in **Fig. 3 of Wach:**

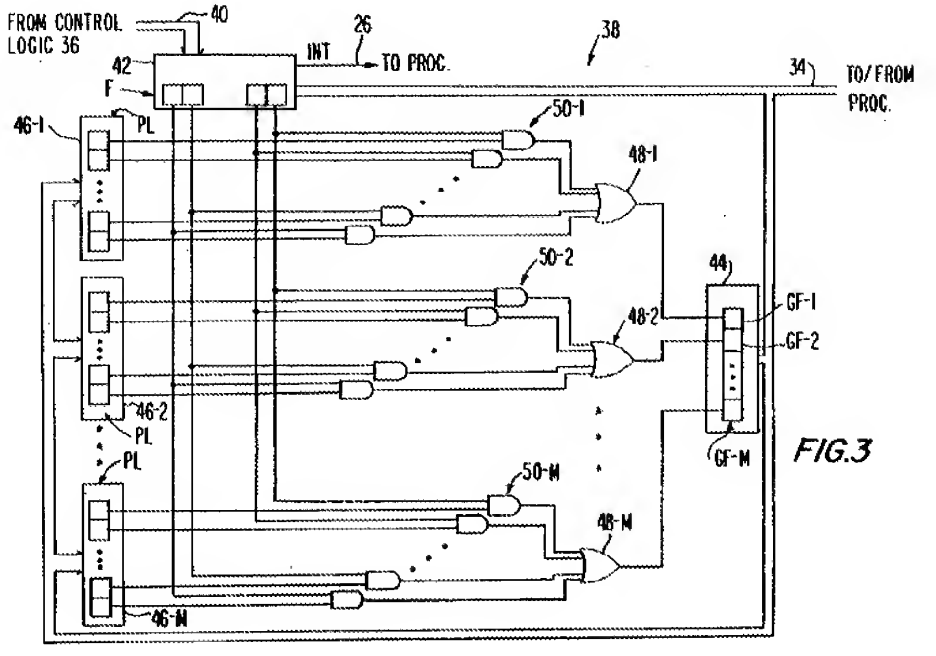

FIG.3

It is clear from at least Fig. 3 of Wach, a logical OR is arranged to indicate, to the locations GF or interrupt inputs of the interrupt controller 44 of the interrupt manager 38, the presence of a corresponding interrupt request signal from at least one output of a plurality of logical AND gates.

Applicants' other arguments are moot in view of the new ground of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Khanh Dang/

Primary Examiner, Art Unit 2111